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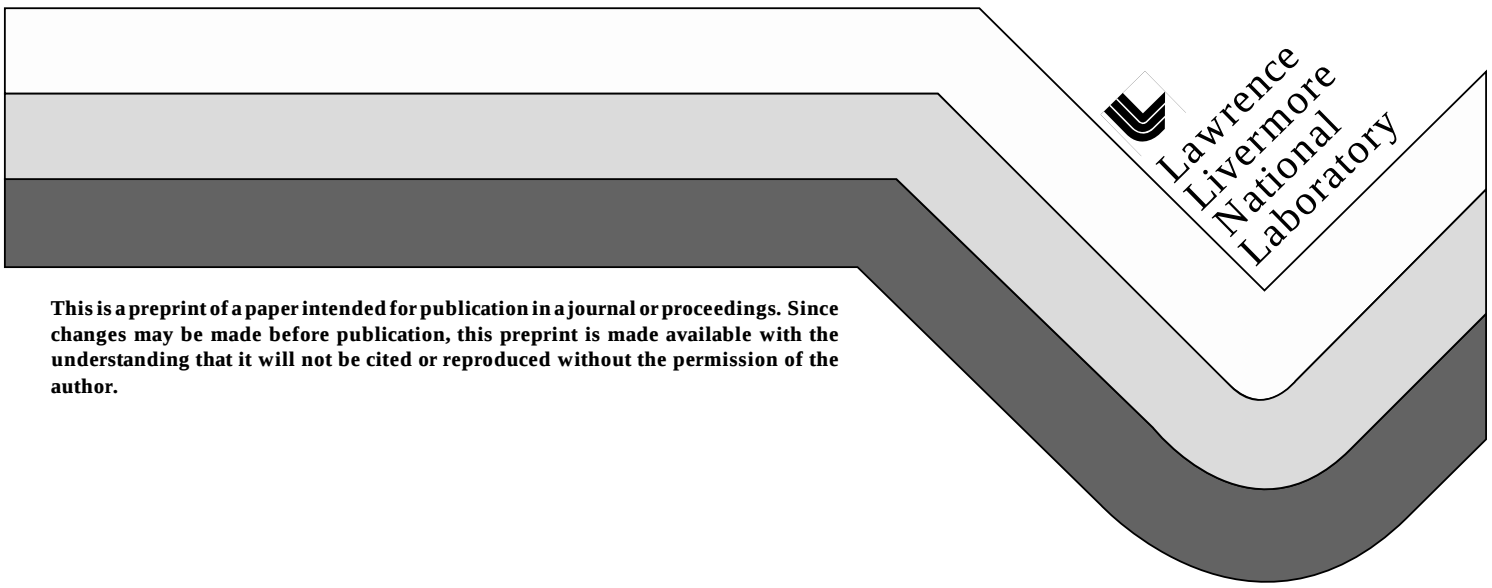

Single Event Effects and Performance Predictions for Space Applications of RISC Processors

J. R. Kimbrough[1], N. J. Colella[1], S. M. Denton,[1] D. L. Shaeffer[1], D. Shih[1], J. W. Wilburn[1],
P. G. Coakley[2], C. Casteneda[3], R. Koga[4], D. A. Clark[5], J. L. Ullmann[5]
[1]Lawrence Livermore National Laboratory*, Livermore, CA 94550, [2]JAYCOR, San Diego, CA 92121,
[3]Crocker Nuclear Laboratory, Davis, CA 95616, [4]The Aerospace Corporation, El Segundo, CA 90245,
[5] Los Alamos National Laboratory, Los Alamos, NM 87545

ABSTRACT

Proton and ion Single Event Phenomena (SEP) tests were performed on 32 bit processors including R3000As from all commercial manufacturers along with the Performance PR3400 family, Integrated Device Technology Inc. 79R3081, LSI Logic Corporation LR33000HC and Intel i80960MX parts. The microprocessors had acceptable upset rates for operation in a low earth orbit or a lunar mission such as CLEMENTINE with a wide range in proton total dose failure. Even though R3000A devices are 60% smaller in physical area than R3000 devices there was a 340% increase in device Single Event Upset (SEU) cross section. Software tests of varying complexity demonstrate that registers and other functional blocks using register architecture dominate the cross section. The current approach of giving a single upset cross section can lead to erroneous upset rates depending on the application software.

INTRODUCTION

The rapid performance increase in commercial microprocessors continues to outstrip the performance of hardened microprocessors. This performance growth and the need for more computational power in

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satellites without an accompanying increase in cost, volume, mass and power consumption suggests the use of commercial parts with appropriate parts screening and quality control.

Lawrence Livermore National Laboratory (LLNL) developed RISC (Reduced Instruction Set Computer) systems for use as embedded controllers capable of multi-processor operation for satellite applications [1]. The original 20 MIPS (Million Instructions Per Second) system based on the R3000 processor and R3010 floating point accelerator was replaced with a second generation computer based on 79R3081E microprocessor. The computer system's main memory incorporated Error Detection And Correction (EDAC) to provide double bit error detection and single bit error correction.

This paper describes the proton and ion Single Event Upset and Single Event Latchup (SEU/SEL) radiation testing and results for R3000As, Performance Semiconductor Inc. (PSI) PR3400 family, LSI Logic Corporation (LSI) LR33000HC, Integrated Device Technology Inc. (IDT) 79R3081E processors and Intel (INC) i80960MX. The R3000As based on MIPS architecture were from IDT, LSI, PSI, NEC; and Siemens Components, Inc. (SCI). Device markings are shown in Table 1.

Table 1. Manufacturer and device markings

Maker	Device Markings	Device Technology
IDT	79R3000AE-25G144 9105M &79R3000AE-25G144 9128CP	0.8 µm CMOS 6
LSI	LR3000AHC-25 MIPS CPU TAC 9130 C3504-N ENG	0.7 µm CMOS
LSI	LR3000AH-25 MIPS CPU C33663.22 TAC 91263	0.7 µm CMOS
NEC	D30310R-33 VR3000A-33 9143E9 CPU	CMOS
PSI	PR3000A-25PGC 9034 V3 & PR3000A-25GAC 9143 V3	0.6 µm PACE III CMOS
SCI	SABR3000A-33-AE S10420890R	CMOS
PSI	PR3400-33SG175C 9205 & PR3400-33SG175C 9218	0.6 µm PACE III CMOS
PSI	PR3400A-25PGC 9051 & PR3400A-25SG145C 9130	0.7 µm PACE II CMOS
PSI	PR3400L-33SG145C 9214 & PR3400L-33SG145C 9219	0.6 µm PACE III CMOS
IDT	79R3081E-25 9219C & 79R3081E-25 9222C	0.8 µm CMOS 6
LSI	LR33000HC-25 MIPS CTRLR C36618.5 NAC 9207	1.0 µm CMOS
INC	MG80960MX-16 Q310 SAMPLE	1.0 µm CMOS III

The MIPS Computer Systems R3000A integrated circuit mask set represents a 60% physical size reduction of the original MIPS R3000 [2]. The R3000A is a 32 bit RISC microprocessor made up of two on-chip processors. The Central Processor Unit (CPU) is 32 bit processor with a five stage instruction pipeline allowing the execution rate to approach one instruction per cycle. The system control coprocessor (CPO) contains the exception/control registers, memory management registers, interfaces to both external data and instruction caches, and the 64 entry Translation Lookaside Buffer (TLB).

The Performance Semiconductor, Inc. PR3400 family of devices combines the Floating Point Accelerator with the R3000/R3000A processor. The devices tested included the PR3400A, PR3400 and PR3400L. The PR3400A contained separate die for the R3000A processor and R3010A floating point accelerator. The processor and floating point accelerator were combined into one die in the PR3400 and PR3400L. The PR3400 contains a clock generator that only requires one external clock input rather than the 4 clock inputs required by the R3000A and PR3400L.

The LSI Logic Corporation LR33000HC processor based on the R3000 is intended for imbedded applications. The CPO found on the MIPS R3000/R3000A architecture was eliminated. The exception and control registers were moved to the CPU and two hardware breakpoint registers were added to aid debugging. The external data and instruction caches were replaced by an on-chip 8 kbytes instruction and 1 kbytes data caches. In addition the device contains 3 timers/counters, a DRAM (Dynamic Random Access Memory) controller, a one deep write buffer and requires only one external clock input.

The Integrated Device Technology, Inc. 79R3081E processor combines the Floating Point Accelerator with the R3000A on a single chip. The on-chip caches consist of 16 kbytes instruction cache and 4 kbytes data cache which the user can configure as 8 kbytes instruction and data caches with parity protection. The chip also has 4 deep read/write buffers, DMA (Direct Memory Access) arbiter and a external clock input.

The Intel i80960MX is a second generation military version of the i960 embedded microprocessor and implements the Extended Architecture of the Joint Integrated Avionics Working Group. On-chip the i80960MX contains the central processor, floating point unit, memory management unit, 2 kbytes instruction

cache, 2 kbytes data cache and interrupt controller. Combining RISC technology and superscalar architecture the i80960MX can execute three instructions per clock cycle. The self test function built into the i80960MX which tests 85% of the internal logic was used to test for device upsets.

TEST SETUP

Figure 1 shows the test setup. To accommodate the variety of MIPS microprocessors four different test boards with the tests stored in on board EEPROM (Electrically Erasable Programmable Read Only Memory) are used to test MIPS based devices. R3000 and R3000A testing was performed on DMS (Data Management System) boards developed at LLNL [3]. Some R3000A and all the PR3400 family was done on a LLNL development board incorporating the LSI RPM3330E NGINE board. The IDT 3081E was tested on an IDT evaluation board. The LR33000HC was tested on the LR33000HC Pocket Rocket Evaluation Board from LSI Logic. In all cases the Sun computer displayed and stored the upset information required for upset cross section calculations. The original test board communicates to the Sun via a digital I/O port, but the other boards use RS232C. The communication link provides a continuous real time display of processor status. This continuous display indicates when an upset or latchup occurs. A slower data acquisition program built around LabVIEW [4] monitors the test board voltage, current, temperature of device under test and up to three other temperatures. The LabVIEW CAMAC/Macintosh data acquisition system graphically displays the data, and writes the data onto the disk every one to five seconds to avoid loss of data if the system fails.

The separate test setup for the Intel i80960MX maintains the environmental monitor section of the test setup and replaces the SUN computer system with counters and timers. The i80960MX test board cycles the microprocessor in a continuous self-test and the number of test loops, failures and time to complete a test are displayed.

Determining the cross section of a processor is complicated by device architecture and test software. Physically the microprocessor is made of different functional blocks with varying architecture. The cross section is dependent upon how extensively the software checks the functional blocks. Ideally the test

software should be similar to the final application in the use of functional blocks and execute at application software clock speed. To achieve these goals, our test method is based upon Koga's "Self-testing single computer method," which is dynamic testing of the processor's functional blocks [5].

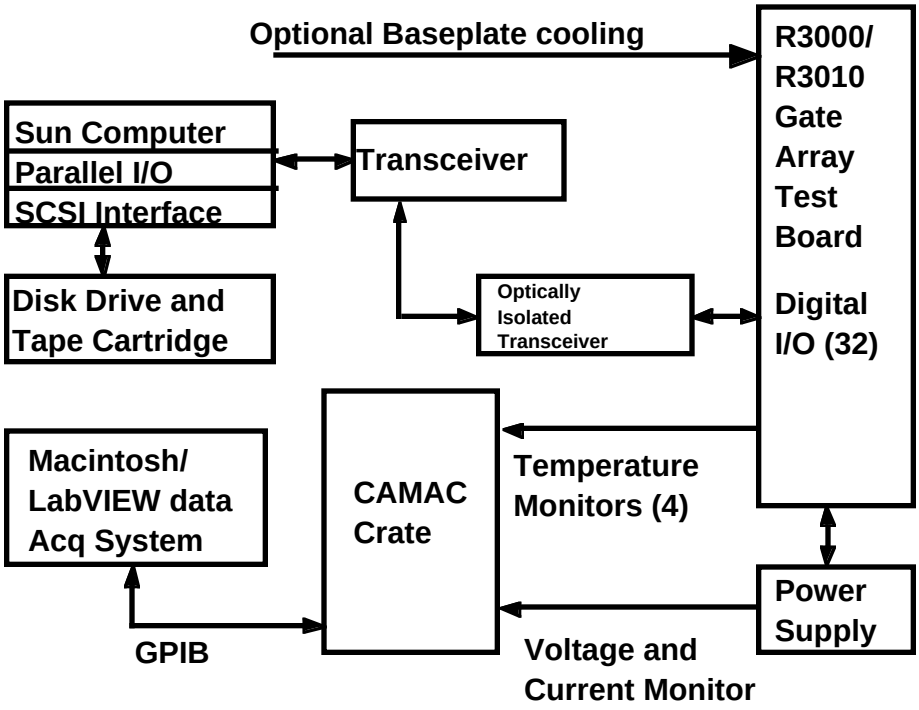

Figure 1. Processor Test Setup

The test software consist of three separate programs that range from a simple register test to extensive tests on the entire microprocessor. The "Register Test " compares 12 of the 32 general purpose registers. In execution it performs one compare each clock cycle and continuously loops through the 12 registers.

The "CPU Test" was the original code used in our proton tests at Los Alamos Meson Physics Facility (LAMPF) [3]. The CPU Test tests the following percentages of instructions: 50% of the external interface, 33% of the master pipeline and external unit register, and 17% of the address unit instructions. Only six of the 32 general purpose registers are tested and none in the TLB.

The most stringent test, called "Stress Test," is designed to approximate the instruction set and addressing required by flight software. The Stress test exercises: 50% of the external interface, 75% of the master pipeline control and external unit register, 100% of the address unit, 17% of the system coprocessor,

100% of the TLB and all the general purpose registers. The program was modified to eliminate testing nonexistent features, such as the TLB in the LR33000HC and 79R3081E, and no testing was done of on-chip caches in the LR33000HC and 79R3081E. All cross section graphs are based on Stress test data unless labeled otherwise.

All these devices are bottom cavity mounted which places the exposed die closest to the circuit board. A right angle adapter was made to raise the device from the circuit board and expose the die to beam without first going through the wafer.

Device SEU cross section is calculated by summing the upsets and fluence at each energy or LET for the specific device types from each manufacturer. The device upset cross section calculation is shown in equation 1. The fluence is in protons per cm^2 or ions per cm^2.

$$\sigma = \frac{\sum \text{Upsets per device}}{\sum \text{Fluence per device}} \qquad (1)$$

The major sources of uncertainty in σ are the fluence and the statistics for a small number of upsets. The limited number of upsets and poor statistics is the dominate contribution to the uncertainty. Therefore the standard deviation in the cross section is calculated using equation 2, which ignores the 5% or less uncertainty contribution of the beam fluence measurement.

$$\text{Error} = \frac{(\sum \text{Upsets per device})^{0.5}}{\sum \text{Fluence per device}} \qquad (2)$$

TEST FACILITIES

SEU tests were performed using both 24 and 60 MeV protons at beam line number two of the variable energy isochronous cyclotron at the Crocker Nuclear Laboratory of the University of California at Davis. The beam line is dedicated to proton SEU experiments and equipped with an automated beam current monitor system. The current monitoring is done with a Faraday cup and a secondary electron emission monitor (SEEM) [6]. Total dose and deposited proton energy calculations took into account the 18 mil Kovar lid on the processors [7]. Aluminum barriers reduced the proton energy to 24 MeV. The proton

beam flux is highly uniform out to 7 cm diameter and then drops rapidly. A 3.5 inch thick Delrin block was used to collimate the beam on to the device under test.

Tests using 256 and 800 MeV protons were done at the Weapon Neutron Research beam line at the Los Alamos Meson Physics Facility [3]. The beam spot is approximately a two dimensional Gaussian profile with a full-width-half-maximum of one inch. Due to high energy and corresponding large penetration range, no collimators were used for either of these energies. A dual beam laser alignment system was used to position the device under test. The beam spot size and location were confirmed by use of a fluorescent target and film mounted at the device location. The dosimetry is based on radioactivation analyses of the gamma decay from irradiated aluminum disks placed on the test fixture.

Ion SEP tests were performed in the Aerospace Corporation target and diagnostic chamber on the 88 inch cyclotron at Lawrence Berkeley Laboratory [8]. Aerospace Corporation provided the monitoring for ion flux and energy. All devices were delidded and had a zero degree angle between beam and the normal to the chip surface. Ion characteristics are shown in Table 2.

PROTON SEP RESULTS

All devices underwent low energy proton SEU stress tests and a down selection was done to determine R3000As and combinational devices for 256 MeV and 800 MeV proton SEU stress tests. The down select was based on proton total dose failures, ion latchup and programmatic interests. The subset of R3000As consisted of LSI, Performance and Siemens devices. The combinational devices were: PR3400, PR3400L and 79R3081E. The individual data points and error bars were plotted and then curve fitted using the single point Bendel "A" parameter [9]. Each data point represents the cross section and standard deviation as calculated by equations 1 and 2. Error bars representing the standard deviation are shown except when only a single measurement point was taken. Previous R3000 SEU measurements demonstrated that the SEU cross section is essentially independent of proton flux over our test range of 10^7 to $3x10^{10}$ (cm^{-2}-s^{-1}) [10]. Figure 2 is a summary of R3000A data and "A" parameter curve fits. Error bars, "A" parameters, and curve fits for R3000As from each manufacturer are shown in figures 3 and 4. At 800 MeV

the measured cross sections of Performance, LSI and Siemens R3000As have an average value of 5.1×10^{-10} ± 0.2 cm^2/device.

Despite a 60% reduction in die area, the R3000A cross section is a factor of 3.4 ± 0.3 larger than the R3000 cross section as shown in Table 3 [10]. Apparently, the reduction in the physical sensitive area is more than offset by lower critical charge required to cause an upset.

Table 2. Characteristics of Ions Used in SEP Tests

Ion	Energy (MeV)	LET (MeV/(mg/cm^2))	Range in Si (μm)
^{15}N	67	2.8	70
^{20}Ne	90	5.5	54
^{40}Ar	180	14.3	47
^{56}Fe	252	24.7	41
^{86}Kr	380	38.5	46
^{136}X	603	63.3	46

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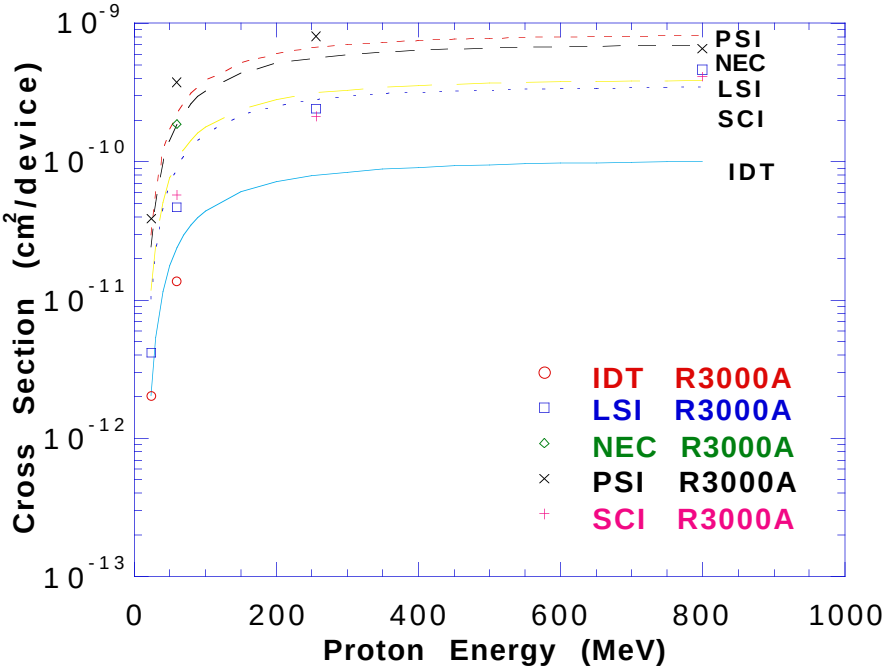

Figure 2. SEU cross section versus proton energy for R3000As

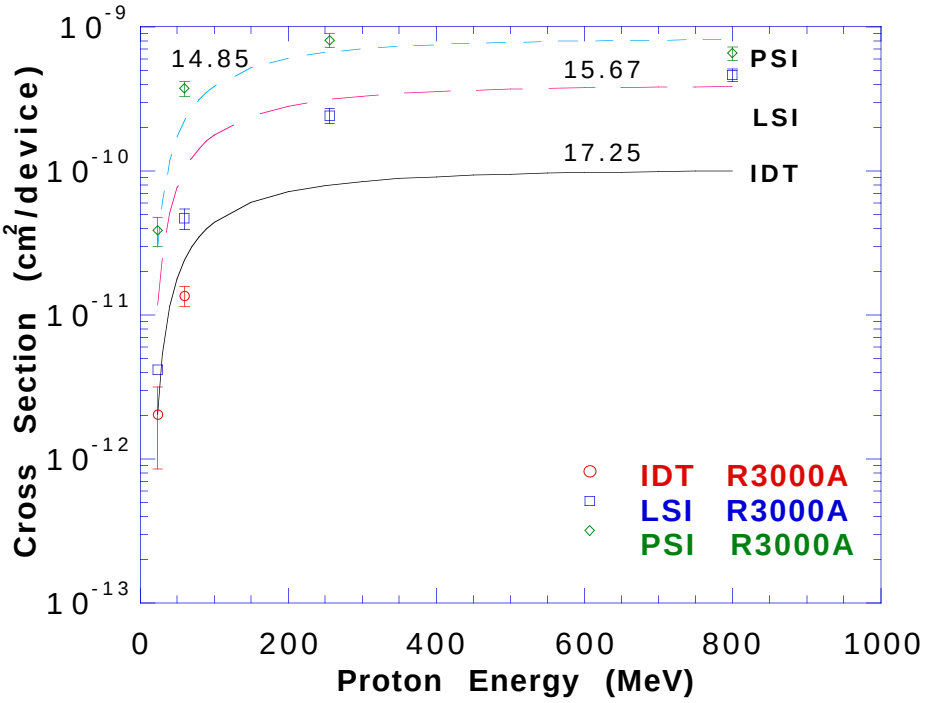

Figure 3. SEU cross section and "A" parameter for IDT, LSI and Performance R3000As

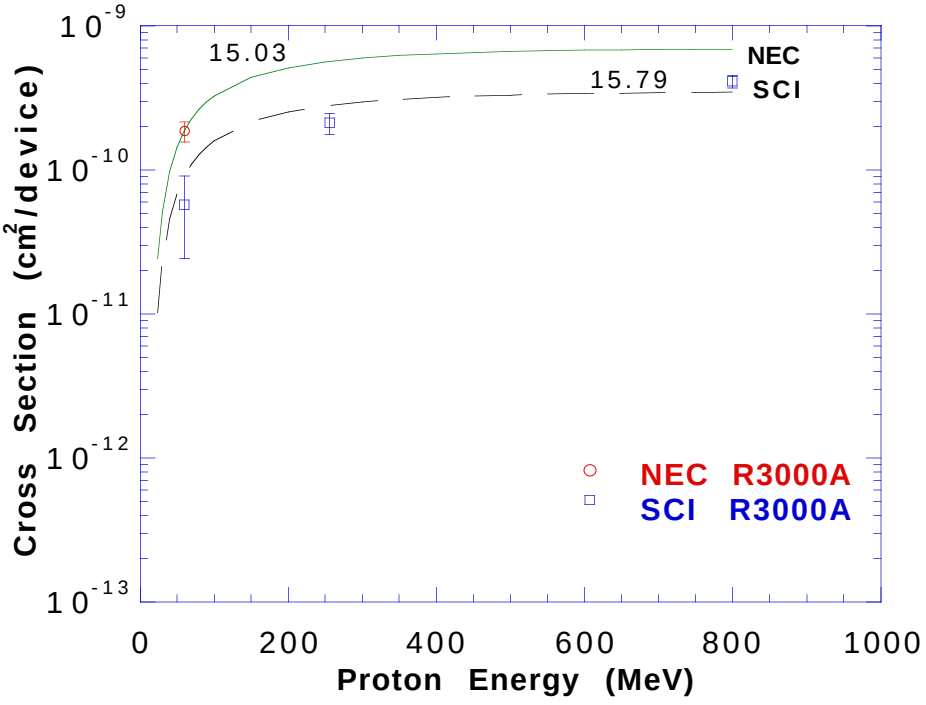

Figure 4. SEU cross section and "A" parameter for NEC and Siemens R3000As

The PR3400A has the largest cross section at all energy levels for the PR3400 family shown in figure 5. This is consistent with the device architecture of separate R3000A and R3010 die in the device while the PR3400 and PR3400L combines all the functions into one die.

Despite different architecture and tests the 79R3081E and i80960MX had similar cross sections, approximately 3 times larger than the simplest device, the LR33000, as shown in figure 6. However the 79R3081E had nondestructive current latchups at 256 and 800 MeV. In several cases the current jumped up in stages until eventually the device stopped operating, as shown in figure 7. After cycling the power the device resumed operation.

Devices from each manufacturer were irradiated to failure during low energy proton SEU tests. Total dose failure points per device type are shown in figure 8. The single Siemens part failed at 15 krad(Si) while the LSI LR33000HC was functional at 1224 krad(Si). Only the Performance Semiconductor PR3400 failed to recover.

Table 3. Comparison of R3000 and R3000A Device Cross Sections for 60 MeV Protons

Company	R3000 Cross Section (cm^2/device)	R3000A Cross Section (cm^2/device)	Ratio of Cross Section R3000A/ R3000
IDT	Latched	1.36×10^{-11}	
LSI	1.54×10^{-11}	4.65×10^{-11}	3.0 ± 0.2
NEC	Not Tested	1.85×10^{-10}	
PSI	1.16×10^{-10}	3.70×10^{-10}	3.2 ± 0.1
SCI	1.46×10^{-11}	5.7×10^{-11}	3.9 ± 0.7

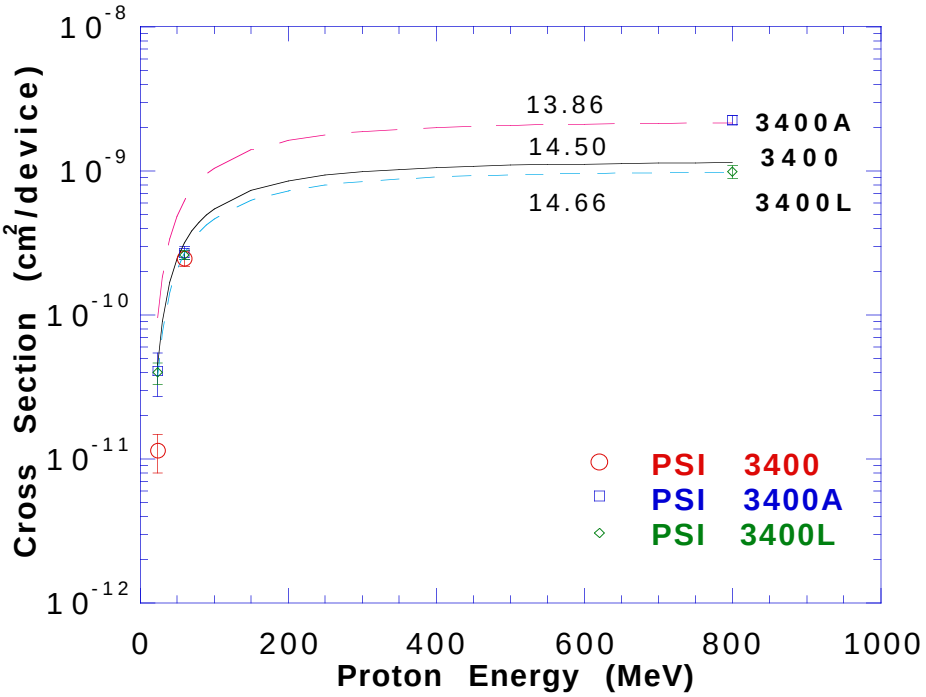

Figure 5. SEU cross section and "A" parameter for Performance 3400 family

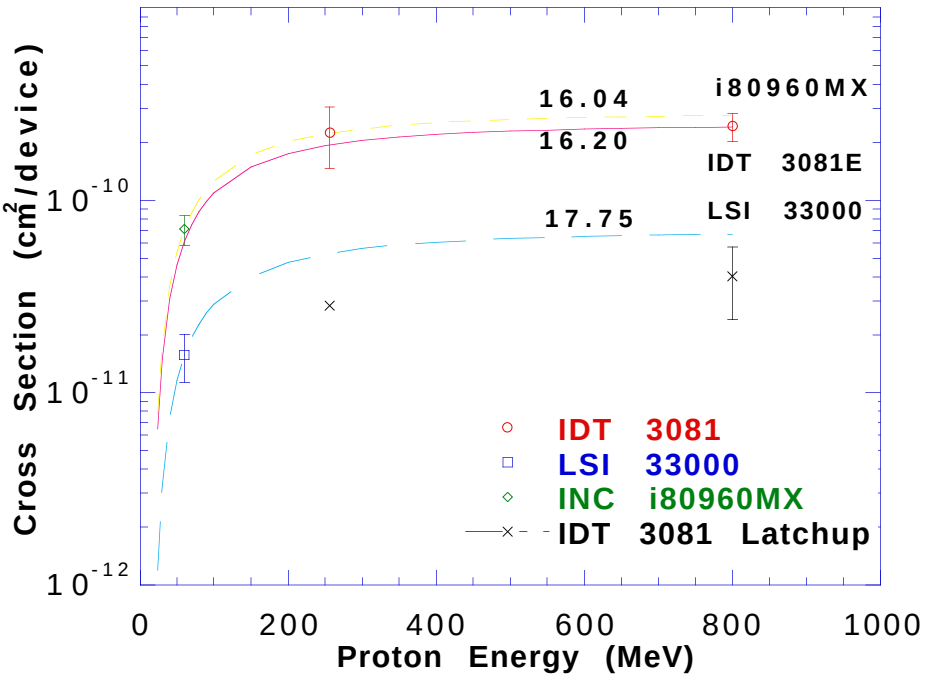

Figure 6. SEU cross section and "A" parameter for IDT 3081E, LSI LR33000HC and i80960MX

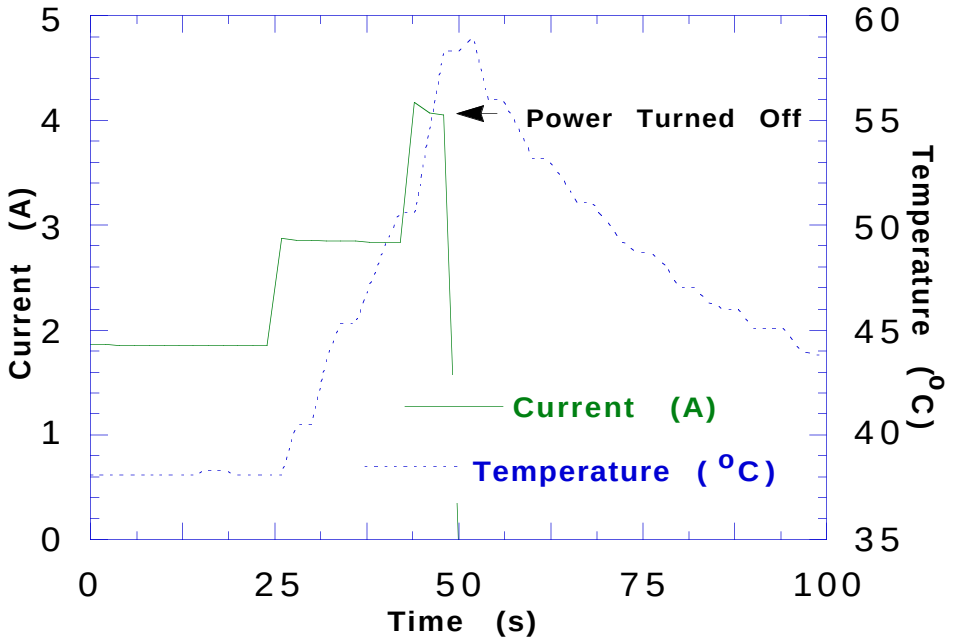

Figure 7. Supply current and CPU temperature for the IDT 3081 latchup during 256 MeV proton SEU tests

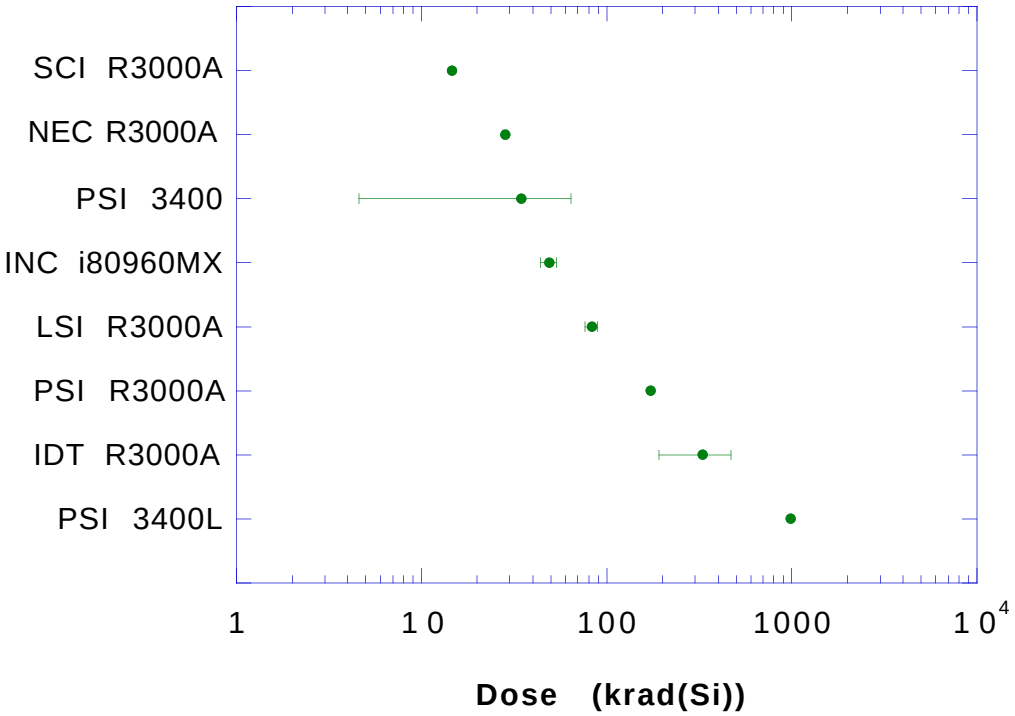

Figure 8 Total dose failure point during proton SEU tests

ION SEP RESULTS

The heavy ion SEP stress tests were done on R3000As, the PR3400 family and LSI LR33000HC. Figures 9 and 10 show R3000As from all manufacturers and PR3400 family. Each data point represents the cross section and standard deviation as calculated by equations 1 and 2. Error bars representing the standard deviation are shown except when only a singe measurement point was taken.

Figures 11-15 show the cross section and LET for IDT, LSI, NEC, Performance, and Siemens R3000A microprocessors. No cross section was calculated for the NEC R3000A at 63.3 (MeV/mg/cm^2) due to current latchup. Despite wide variations in R3000A cross sections shown at lower LET below 25 (MeV/mg/cm^2) the device saturated cross section averaged $1.35 \times 10^{-3} \pm 0.011 \times 10^{-3}$ cm^2/device at 63.3 (MeV/mg/cm^2) for IDT, LSI, Performance and Siemens R3000A . The apparent maximum cross sections at low LETs for LSI, NEC, Performance and Siemens devices falls within the uncertainty range of two standard deviations and is not due to ion range out.

The wide variation in device sensitivity is shown by the range in threshold LETs. The threshold LET is defined as the LET where the device cross section is 10 percent of the maximum device cross section. The threshold LETs range from 5 to 16 (MeV/mg/cm^2) for Performance and Siemens R3000As. All the Performance parts (R3000A, 3400, 3400A and 3400L) were consistent with a threshold of 5 (MeV/mg/cm^2). This was followed by threshold LETs of 8, 11, 14, and 16 (MeV/mg/cm^2) for R3000As from NEC, LSI , IDT, and Siemens. The LSI 33000 had a threshold 8 (MeV/mg/cm^2).

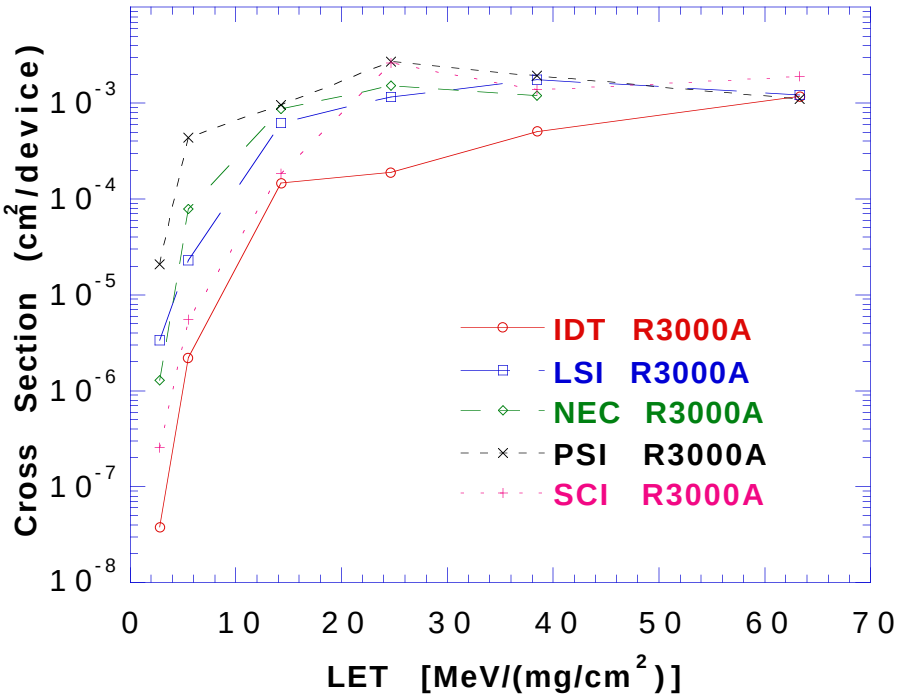

Figure 9. SEU Cross sections for all R3000As

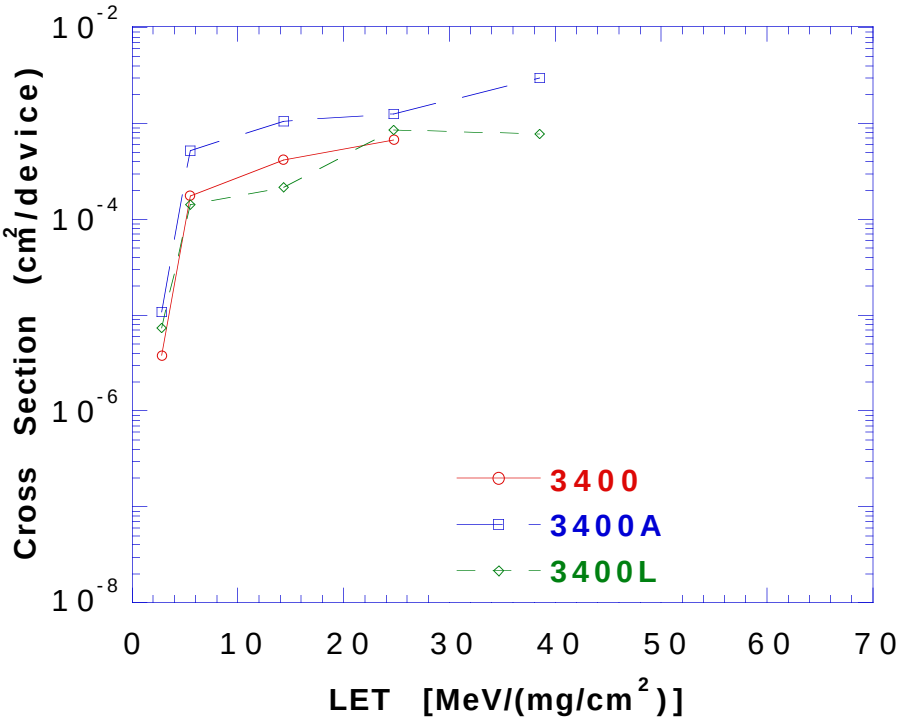

Figure 10. SEU Cross sections for the PR3400 family

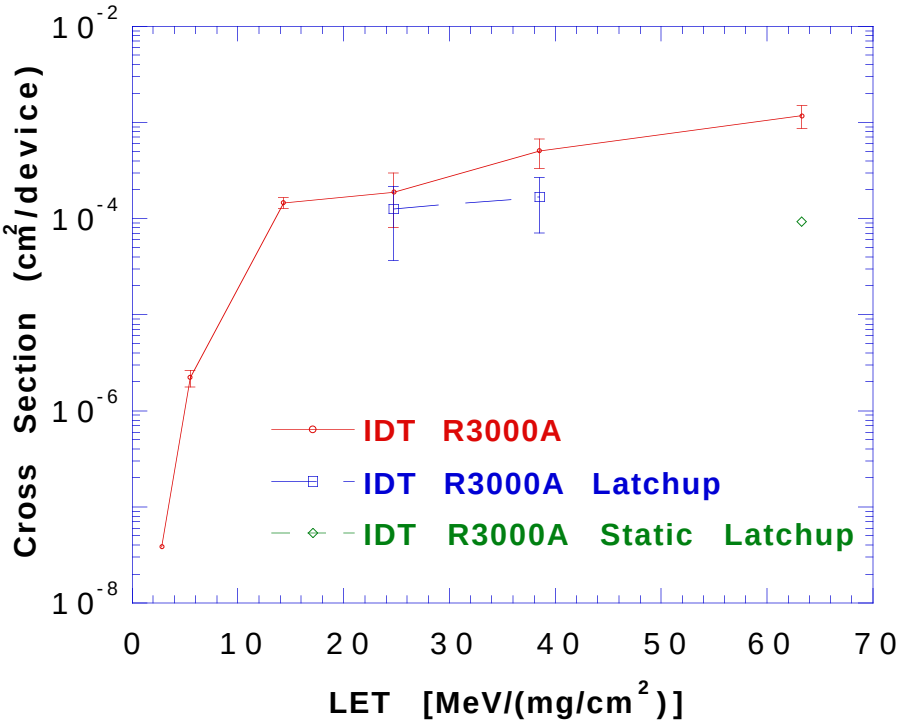

Figure 11. SEU and Latchup Cross sections for IDT R3000A

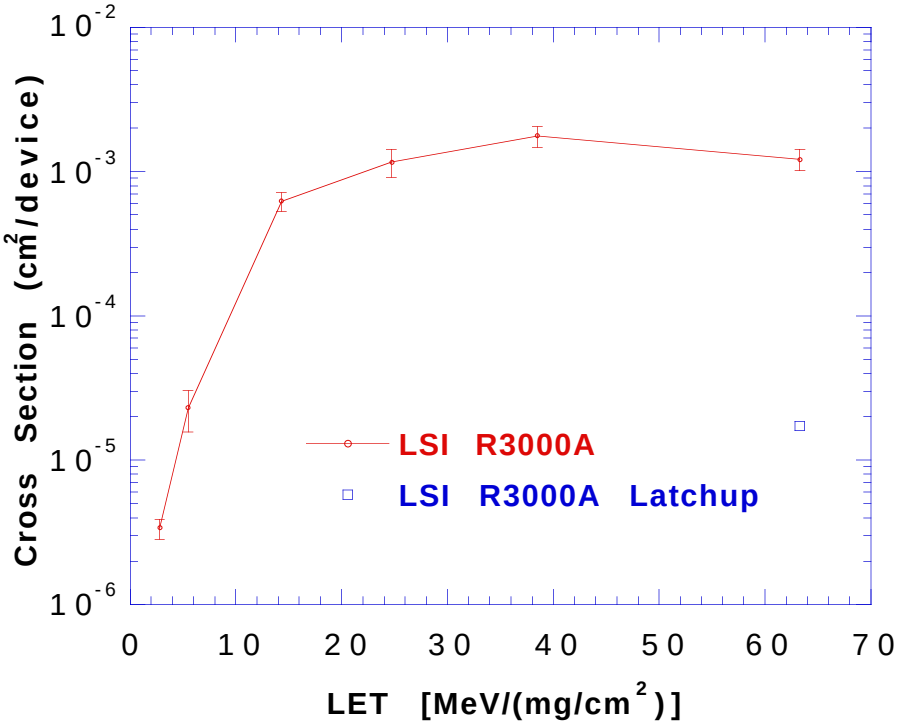

Figure 12. SEU and latchup cross section for LSI R3000A

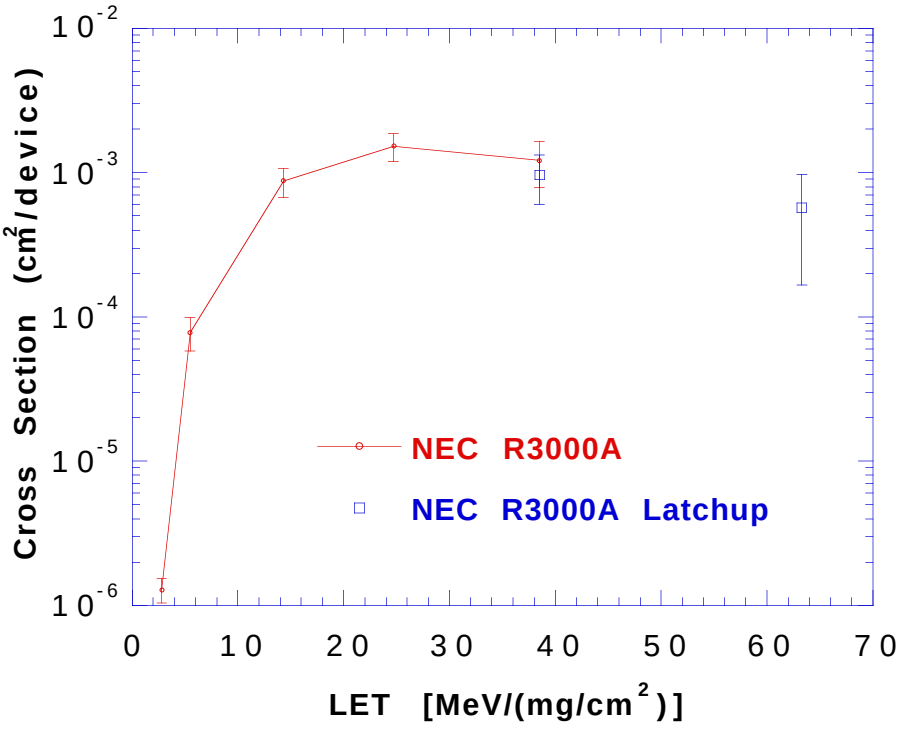

Figure 13. SEU and latchup cross section for NEC R3000A

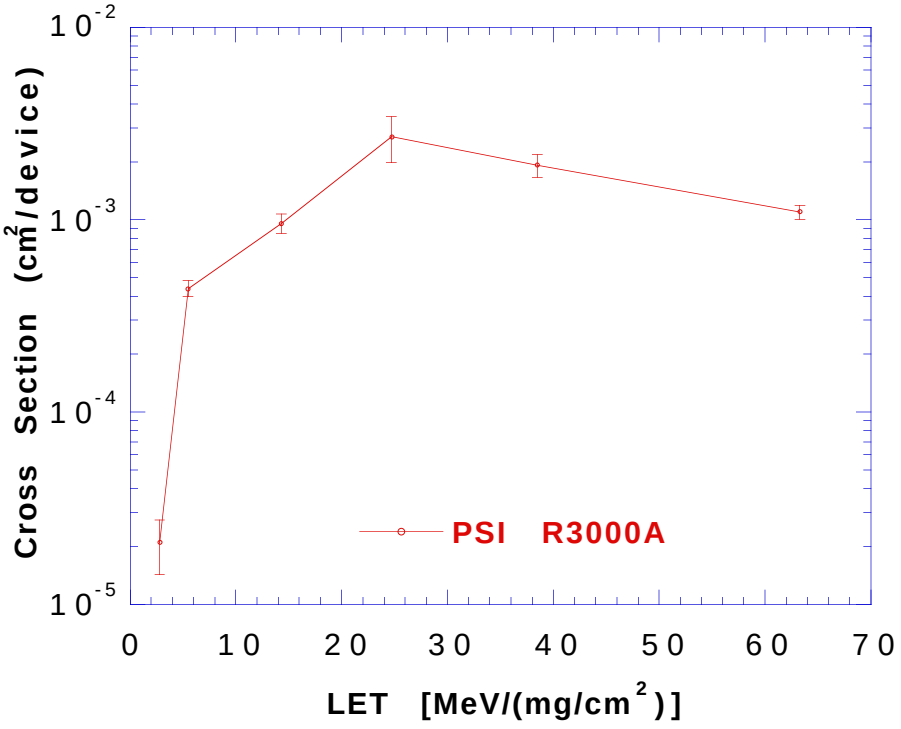

Figure 14. SEU cross section for Performance R3000A

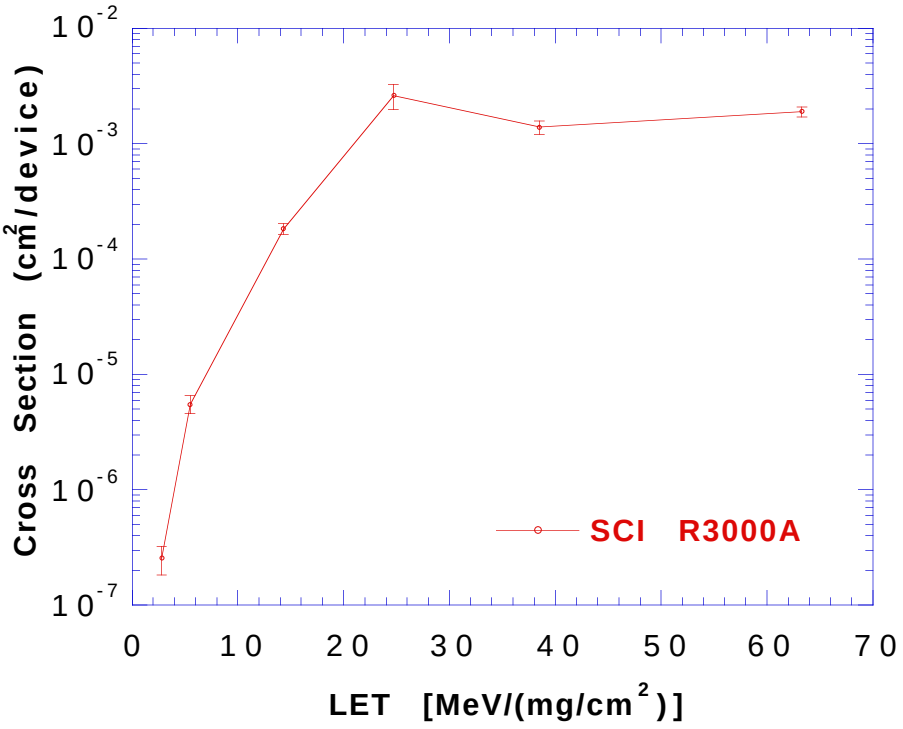

Figure 15. SEU cross section for Siemens R3000A

Figures 16 - 19 show the Performance PR3400 family and LSI 33000 cross sections. PR3400A had the maximum cross section of 2.9×10^{-3} compared to 7.7×10^{-4} for the PR3400L at 63.3 (MeV/mg/cm^2). Testing of the PR3400 ended at 24.7 (MeV/mg/cm^2) due to latchups.

The LSI 33000 maximum cross section is 3.69×10^{-3} at 38.5 (MeV/mg/cm^2). However, only a single upset was obtained for the LR33000HC at LET 38.5 (MeV/mg/cm^2) due to the onset of latchup.

No current latchup occurred for PSI and SCI R3000As. However, current latchup did occur for IDT, LSI, NEC R3000As, and PR3400 family. The onset of current latchup occurred at 24.7, 63.3, 38.5 (MeV/mg/cm^2) for IDT, LSI and NEC R3000As. Figure 20 shows the current and temperature when the NEC R3000A had a current latchup. The latchup threshold for PR3400 and PR3400L occurred at 24.7 (MeV/mg/cm^2). In the case of the PR3400, latchup was destructive. Destructive latchup for the 3400L was at 38.5 MeV/mg/cm^2), as shown in figure 21. The 3400A had a nondestructive latchup at 63 (MeV/mg/cm^2).

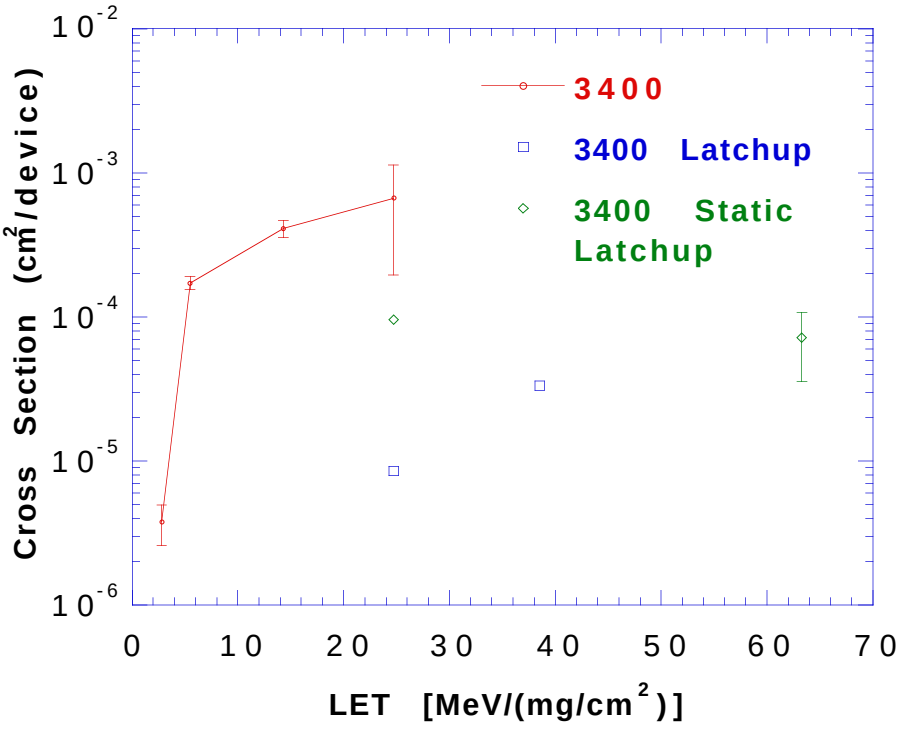

Figure 16. SEU and latchup cross sections for 3400

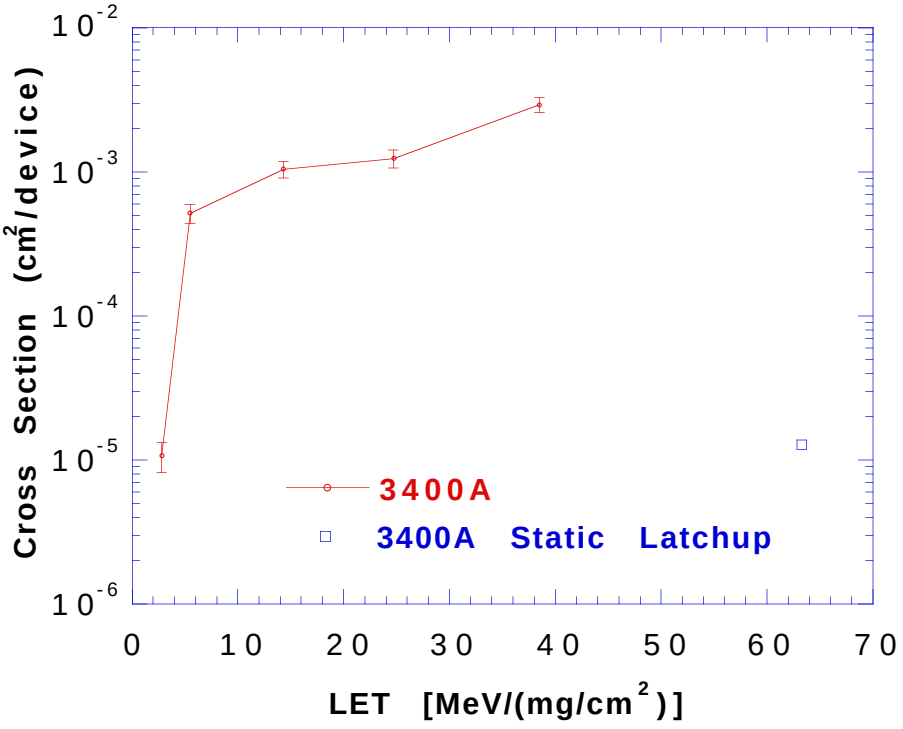

Figure 17. SEU and latchup cross sections for 3400A

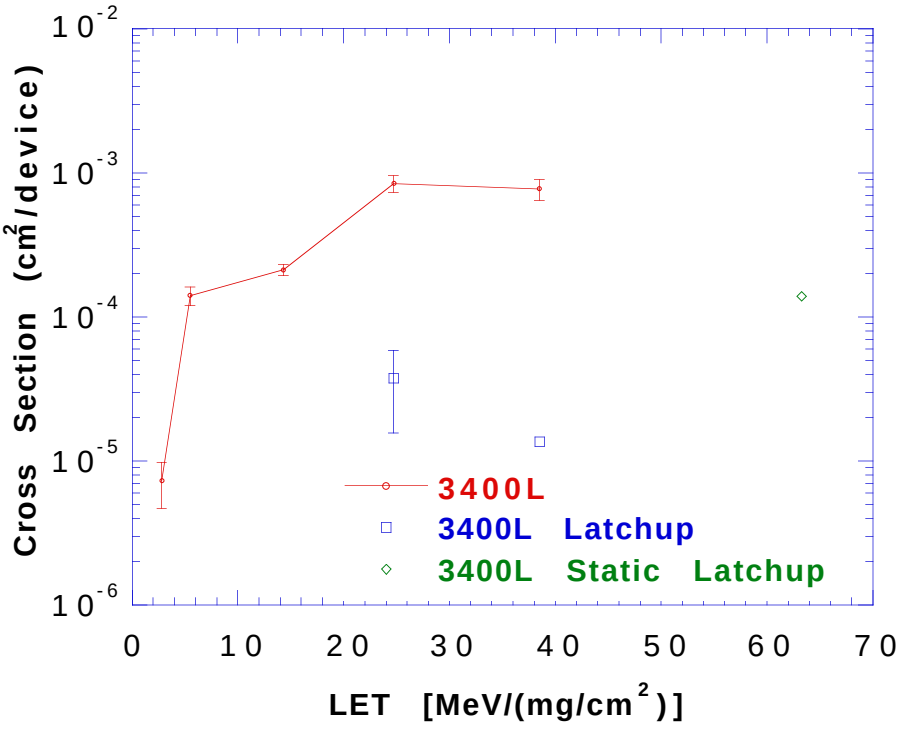

Figure 18. SEU and latchup cross sections for 3400L

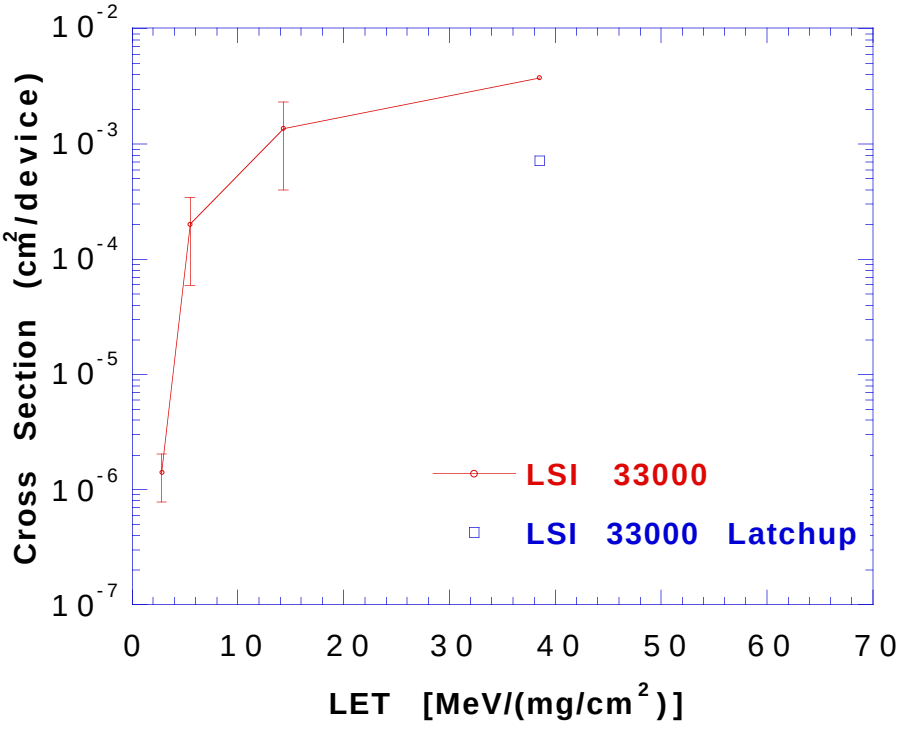

Figure 19. SEU and latchup cross sections for LSI 33000

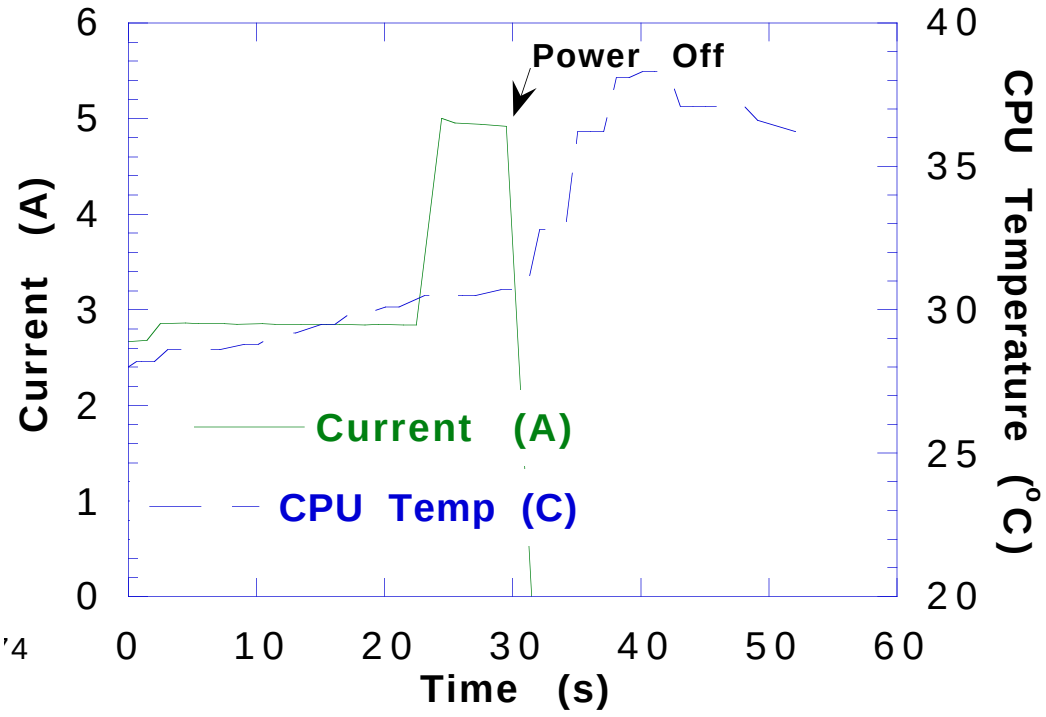

Figure 20. Supply current and CPU temperature for NEC R3000A latchup during Kr SEU tests.

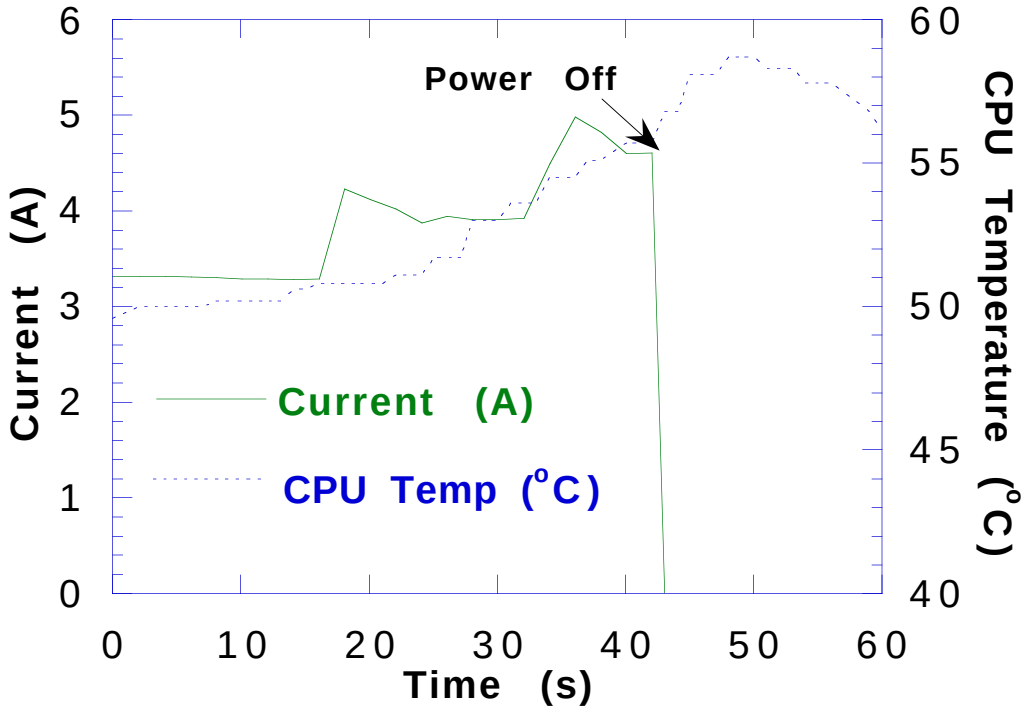

Figure 21. Supply current and CPU temperature for PR3400L latchup during Kr SEU test.

COMPARISON OF TEST PROCEDURES

In order to determine the effect the software test has on the device SEU cross section calculation our tests were compared to each other and to European Space Agency (ESA) cross sections for R3000As [11]. In an effort to correlate the effectiveness of the software tests and the calculated cross section the Stress test, CPU test and Register tests were run on Performance R3000As and 3400L devices. The 60 MeV proton flux was maintained between 10^8 and 10^9 protons/cm^2-s to prevent multiple upsets during a test loop [10]. The results shown in tables 4 and 5 indicate there is no simple correlation between types of software tests. The results do indicate that the memory architecture component of the processor such as the register and TLB dominate the results. This is substantiated by the fact the CPU test with minimal testing of the registers and TLB has the smallest cross section ratio. The fact the CPU to Register ratio is less than one is because the CPU test only checks 6 of the registers while the Register test checks 12 of the registers. The Stress test is the only test to check all of the registers and TLB and should have the largest physical cross section. A complicating issue is that the various tests have different execution times to make one pass through all their checks. The Register test, being the simplest executes 3.9 times faster than the CPU test and 63.5 times faster than the Stress test. The CPU test is 16.2 times faster than the Stress test, which takes 2.94 milliseconds to execute one loop with a 10 MHz system clock.

Table 4. Ratio of SEU Cross Sections for Performance R3000A

Proton Energy	Stress/CPU	Stress/Reg	CPU/Reg
25 MeV	1.0 ± 0.6	0.6 ± 0.5	0.6 ± 0.8
60 MeV	6.4 ± 0.6	2.4 ± 0.3	0.4 ± 0.6

Table 5. Ratio of SEU Cross Sections for Performance 3400L

Proton Energy	Stress/CPU	Stress/Reg	CPU/Reg
25 MeV	10.0 ± 0.7	1.2 ± 0.4	0.7 ±0.9
60 MeV	11.4 ± 0.2	2.6± 0.2	0.3± 0.3

Comparisons among our three software tests and the ESA data shows that different software tests give significantly differently cross sections. We consistently have the larger cross sections for our stress tests than the European Space Agency cross sections[11]. The European Space Agency did a register test looking at 736 bits. The cross section per bit was then multiplied by 736 to get a device cross section to compare with our values. Table 6 shows the ratio of LLNL versus ESA cross sections. We compared our 60 MeV and their 100 MeV results and our 256 MeV with their 200 MeV results. There is a wide range in ratios: however, we consistently have a larger cross section. Thus it is difficult to compare processors based on a single cross section value without knowing how extensive were the software tests.

Table 6. Ratio of LLNL and ESA device cross sections

Manufacturer	Ratio of LLNL/ESA 60/100 MeV	Ratio of LLNL/ESA 200 /256 MeV
LSI	7.43	19.2
PSI	15.2	5.44
SCI		26.1
Average	11.3± 5.5	16.9 ± 10.5

PREDICTED PERFORMANCE IN ORBIT

Upset and Latchup predictions due to protons and ions are calculated using "SPACERAD" [12], for a spacecraft with 60 mils of aluminum shielding in a 500 km orbit with a 60 degree inclination. The IGRF85 magnetic field model is used in both Galactic Cosmic Ray and trapped proton environment. The trapped proton environment is a solar minimum (Sawyer & Vette). The proton upset rate shown in Table 7 is calculated by curve fitting the data to determine the "A" parameter [10].

Adam's solar minimum is used as the space environment for calculating ion upset and latchup rates in Table 8. The ion upset rate is based on the critical LET and the maximum device cross section. For all devices the device depth and funnel length are 2 microns. The critical LET is defined as the LET where the

device cross section is 25% the maximum device cross section. A best case and worst case latchup rate is calculated. The worst case latchup rate is uses the LET prior to the onset of latchup and the best case latchup rate uses the LET and device cross section at the onset of latchup.

Table 7. Proton Upset Rate per Device

Device	A Parameter	Upsets/day
LSI R3000	17.91	3.3×10^{-5}
PSI R3000	16.85	8.0×10^{-5}
IDT R3000A	17.25	5.7×10^{-5}
LSI R3000A	15.67	2.3×10^{-4}
NEC R3000A	15.03	4.2×10^{-4}
PSI R3000A	14.85	1.6×10^{-5}
SCI R3000A	15.79	2.1×10^{-4}
PSI 3400	14.50	7.1×10^{-4}
PSI 3400A	13.86	1.4×10^{-3}
PSI 3400L	14.66	6.1×10^{-4}
IDT 3081E	16.20	1.4×10^{-4}
IDT3081E Latchup	19.3	1.1×10^{-5}
LSI 33000	17.75	3.7×10^{-5}
INC i80960MX	16.04	1.6×10^{-4}

Table 8. Galactic Cosmic Ray Upset Rate per Device

Device	Critical LET	Latchup LET	Upsets/ day	Worst Case Latchups/day	Best Case Latchups/day
IDT R3000A	31	24.7	2.0×10^{-5}	1.4×10^{-5}	4.0×10^{-6}
LSI R3000A	14	63.3	1.8×10^{-4}	4.7×10^{-8}	1.0×10^{-8}
NEC R3000A	11	38.5	2.0×10^{-4}	2.2×10^{-6}	4.8×10^{-7}
PSI R3000A	10	> 63.3	5.7×10^{-4}		
SCI R3000A	20	> 63.3	1.2×10^{-4}		
PSI 3400	6	24.7	4.0×10^{-4}	2.3×10^{-6}	4.4×10^{-7}
PSI 3400A	10	Note A	6.1×10^{-4}	3.2×10^{-8}	6.9×10^{-9}
PSI 3400L	13	24.7	9.8×10^{-5}	2.7×10^{-6}	5.2×10^{-7}
LSI 33000	13	Note B	4.5×10^{-4}	2.5×10^{-6}	8.9×10^{-6}

A) Latchup at LET of 63.3 during static test. B) Latchup at LET of 38.5 during CPU test

CONCLUSION

Proton and ion SEP tests were done on R3000As from all commercial manufacturers along with tests on Performance PR3400 family, IDT 79R3081, LSI LR33000HC and Intel i80960MX parts. The parts had acceptable upset rates for operation in a 500 km 60 degree inclination low earth orbit. The proton total dose failure ranged from 15 to over 1224 Krad(Si) depending upon device type and manufacturer. Even though R3000A devices are physically 60% smaller than R3000 devices there was a 340% increase in device cross section. Software tests of varying complexity demonstrate that registers and other functional blocks using register architecture dominate the cross section. As processors become more complex, it becomes more important to either limit the test to meet the application software requirements or do very detailed tests and break the cross section up into subsets based on functional blocks tested. The current approach of giving a single upset cross section can lead to erroneous upset rate predictions depending on the application software. More work needs to be done in standardizing processor SEU cross section tests.

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Technical Information Department • **Lawrence Livermore National Laboratory**
University of California • Livermore, California 94551